What is claimed is:

[Claim 1] 1. A frequency divider with a 50% duty cycle, comprising:

a bit shifter for outputting a first quotient, a second quotient, and a remainder of the second quotient according to a dividing number;

a counter for counting according to a reference frequency;

a first comparator coupled to the bit shifter and the counter for outputting a first comparison result according to the first quotient and counts of the counter;

a second comparator coupled to the bit shifter and the counter for outputting a second comparison result according to the second quotient and counts of the counter;

a first flip flop coupled to the first comparator and the second comparator for outputting a first result according to the reference frequency, the first comparison result, and the second comparison result;

an AND gate coupled to the bit shifter and the first flip flop for outputting an AND result according to the remainder of the second quotient and the first comparison result;

a second flip flop coupled to the AND gate for outputting a second result according to the AND result and the reference frequency; and

an OR gate coupled to the first flip flop and the second flip flop for outputting a frequency according to the first result and the second result.

[Claim 2] 2. The frequency divider of claim 1, further comprising a reference-frequency generator for outputting a reference frequency.

[Claim 3] 3. The frequency divider of claim 1, wherein the first flip flop is a JK flip flop.

[Claim 4] 4. The frequency divider of claim 1, wherein the second flip flop is a D flip flop.

[Claim 5] 5. The frequency divider of claim 1, wherein the second flip flop is triggered by falling edges of the reference frequency.